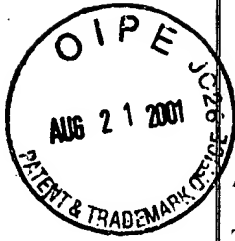


08-23-01

GP/2824



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Eliyahou Harari, Robert D. Norman and Sanjay Mehrotra
 Assignee: SanDisk Corporation
 Title: Flash EEPROM System
 Serial No.: 09/867,836 Filing Date: May 30, 2001
 Docket No.: 11587 M-10187-43C US Group Art Unit: 2824

San Francisco, California
 August 17, 2001

COMMISSIONER FOR PATENTS
 Washington, D.C. 20231

**INFORMATION DISCLOSURE STATEMENT
 UNDER 37 CFR § 1.97(b)**

Dear Sir:

The following Forms 1449 (six sheets) are being filed herewith as an Information Disclosure Statement. Since the references listed on the enclosed Forms 1449 were previously filed in parent patent application Serial No. 08/771,708, now patent no. 5,991,517, no copies are included. Should copies be desired, the undersigned attorney would be glad to furnish them.

**EXPRESS MAIL
 LABEL NO:**

EL707911650US

Respectfully submitted,

Gerald P. Parsons
 Gerald P. Parsons
 Reg. No. 24,486

Aug. 20, 2001
 Date

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Serial No. 09/867,836



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#3/IDS

Applicant(s): Eliyahou Harari, Robert D. Norman and Sanjay Mehrotra
Assignee: SanDisk Corporation
Title: Flash EEPROM System
Serial No.: 09/867,836 Filing Date: May 30, 2001
Docket No.: 11587 M-10187-43C US Group Art Unit: 2824

San Francisco, California
August 20, 2001

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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Dear Sir:


Being filed herewith is a one-page form PTO 1449 listing six Japanese patent publications and one U.S. patent. The Japanese patent publications have been cited in Japanese patent application no. H2(1990)-506478 that is a counterpart to the present application. Japanese patent publication no. 62-188100 has been cited as the primary reference. The cited U.S. patent is a parent to the present application, with claims directed to very similar subject matter. Copies of these references are being filed herewith.

Consideration of each of these references, and the making of them of record in the present application, are respectfully requested.

EXPRESS MAIL
LABEL NO:

EL707911650US

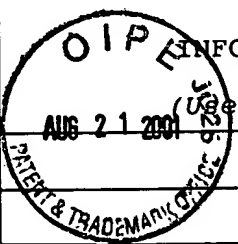
Respectfully submitted,

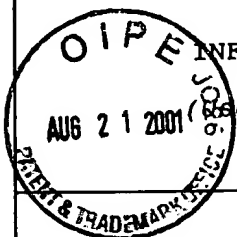

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FORM PT01449 (REV. 8-83)		U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 11587 M-10187-43C US		SERIAL NO. 09/867,836							
<div style="text-align: center;">  </div> <p style="text-align: center;">INFORMATION DISCLOSURE STATEMENT</p> <p style="text-align: center;">(Use several sheets if necessary)</p>				APPLICANT Eliyahou Harari et al.									
				FILED May 30, 2001		GROUP 2824							
U. S. PATENT DOCUMENTS													
*EXAMINER INITIAL		DOCUMENT NUMBER						DATE	NAME	CLASS	SUB CLASS	FILING DATE	
	A1	4	0	9	0	2	5	8	1978	Cricchi			
	A2	4	1	4	9	2	7	0	1979	Cricchi et al.			
	A3	4	2	7	9	0	2	4	1981	Schrenk			
	A4	4	3	5	7	6	8	5	1982	Daniele et al.			
FOREIGN PATENT DOCUMENTS													
		DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)	
	B1	2	0	6	1	6	5	1 B	1981	United Kingdom			
	B2	5	9	3	1	1	5	8	1984	Japanese Pat. Publica.			YES
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)													
	C1	Torelli et al., "An improved method for programming a word-erasable EEPROM," <i>Alta Frequenza</i> , Vol. LII, No. 6, pp. 487-494, Nov.-Dec. 1983											
	C2	Torelli et al., "Single Chip, 16-Station TV Digital Tuning System," <i>SGS-ATES Technical Note</i> 170, pp. 1-19 (1984)											
	C3	Torelli et al., "PLL2K-PLL Frequency Synthesizer For 30 Programs," <i>SGS-ATES Componenti Electronici SpA</i> , Technical Note 152, pp. 1-16 (1982)											
	C4	Scrocchi et al., "EPM32-Electronic Program Memory System For TV (32 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , Technical Note 153, pp. 1-19 (1982)											
	C5	"EPM 16-Electronic Program Memory (16 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M193A-M193C-M193D, 15 pps, (November, 1981)											
	C6	"EPM-32 Electronic Program Memory (32 Stations)," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M293, 16 pps. (October, 1982)											
	C7	"Single Chip Non-Volatile Station Memory, PCM Remote Control Receiver and Display Driver," <i>SGS-ATES Componenti Electronici SpA</i> , MOS Integrated Circuits/M490-M491, 24 pps. (May, 1983)											
EXAMINER									DATE CONSIDERED				
<p>* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>													

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PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
11587 M-10187-43C USSERIAL NO.
09/867,836

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Eliyahou Harari et al.

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A5	4	5	9	9	7	0	7	1986	Fang			
	A6	4	7	1	8	0	4	1	1988	Baglee et al.			
	A7	4	7	6	3	3	0	5	1988	Kuo			
	A8	4	8	0	5	1	5	1	1989	Terada et al.			
	A9	4	8	1	1	2	9	4	1989	Kobayashi et al.			
	A10	5	0	5	3	9	9	0	1991	Kreifels et al.			
	A11	5	0	9	5	3	4	4	1992	Harari			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
	B3	6	2	2	5	7	6	9	9	1987	Japan		Abstr

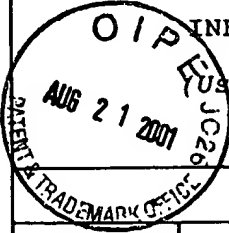
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

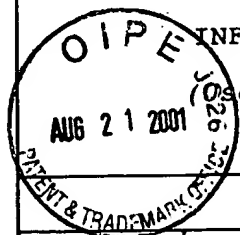
	C8	"PLL TV Microcomputer Interface," SGS-ATES Componenti Electronici SpA, MOS Integrated Circuits/M290, 15 pps. (June, 1982)											
	C9	Gee et al., "An Enhanced 16K E ² PROM," <u>IEEE Journal of Solid State Circuits</u> , Vol. SC-17, No. 5 (Oct. 1982)											
	C10	Torelli, "An LSI technology fully compatible EAROM cell," <u>SGS-ATES Componenti Electronici SpA</u> , 7pp. (1982)											
	C11	Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-28, No. 3, pp. 363-71 (Aug. 1982)											
	C12	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver In A Single Chip," <u>IEEE Digest of Technical Papers</u> , Cat. No. 83CH1872-1, 2pp. (June, 1983)											

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FORM PT01449 (REV. 8-83)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 11587-M-10187-43C US		SERIAL NO. 09/867,836							
 <p>INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)</p>				APPLICANT Eliyahou Harari et al.									
				FILED May 30, 2001		GROUP 2824							
U. S. PATENT DOCUMENTS													
*EXAMINER INITIAL		DOCUMENT NUMBER						DATE	NAME	CLASS	SUB CLASS	FILING DATE	
		A12	4	3	9	3	4	7	5	1983	Kitagawa et al.		
		A13	4	4	1	5	9	9	2	1983	Adlhoch		
		A14	4	4	9	5	6	0	2	1985	Sheppard		
FOREIGN PATENT DOCUMENTS													
		DOCUMENT NUMBER						DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)													
	C13	Torelli et al., "Non-Volatile Station Memory Single Chip Including Remote Control Receiver and Memory Display Driver," <u>IEEE Transactions on Consumer Electronics</u> , Vol. CE-29, No. 3, pp. 103-13 (Aug. 1983)											
	C14	Excerpts from a 1983 Data Book published by SGS-ATES Group, 45 pp. (Nov. 1983)											
	C15	Berenga et al., "E ² -PROM TV Synthesizer," <u>IEEE Digest of Technical Papers</u> , Cat. No. 78CH1298-9SSC, 4 pp. (Feb. 1978)											
	C16	Klingman, "Microprocessor Systems Design," <u>Prentice-Hall, Inc.</u> , pp. 30-31 (1977)											
	C17	Masuoka et al., "A 256-kbit Flash E ² PROM Using Triple-Polysilicon Technology," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 4, (August 1987)											
	C18	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," <u>IEEE Journal of Solid-State Circuits</u> , Vol. SC-22, No. 3 (June, 1987)											
	C19	Krick, P.J., "Three-State MNOS Fet Memory Array," <u>IBM Technical Disclosure Bulletin</u> , Vol. 18, No. 12, pps. 4192-4193 (May, 1976)											
EXAMINER									DATE CONSIDERED				
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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A15	4 8 0 7 1 8 8	1989	Casagrande			
	A16	4 9 5 6 8 1 6	1990	Atsumi et al.			
	A17	4 9 9 9 8 1 3	1991	Ohtsuka et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C20 Alberts, et al., "Multi-Bit Storage Fet EAROM Cell," IBM Technical Disclosure Bulletin, Vol. 24, No. 7A, pps. 3311-3314 (December 1981)

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	A18	4	8	0	9	2	3	1		2/28/89	Shannon et al.			
	A19	4	7	7	9	2	7	2		10/18/88	Kohda et al.			
	A20	4	7	5	2	9	2	9		6/21/88	Kantz et al.			
	A21	4	8	7	0	6	1	8		9/26/89	Iwashita			
	A22	4	6	1	2	6	2	9		9/16/86	Harari			
	A23	4	7	9	9	1	9	5		1/17/89	Iwahashi et al.			
	A24	4	7	3	3	3	9	4		3/22/88	Giebel			
	A25	4	2	5	3	0	5	9		2/24/81	Bell et al.			
	A26	4	4	6	0	9	8	2		7/17/84	Gee et al.			
	A27	5	1	6	3	0	2	1		11/10/92	Mehrotra et al.			
	A28	5	1	7	2	3	3	8		12/15/92	Mehrotra et al.			
	A29	5	6	0	2	9	8	7		2/92	Harari et al.			
	A30	5	2	9	7	1	4	8		3/94	Harari et al.			
	A31	5	0	0	3	5	1	0		3/91	Hamisaki			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A32 4 1 8 1 9 8 0	1980	McCoy			
	A33 4 2 7 2 8 3 0	1981	Moench			
	A34 4 2 8 7 5 7 0	1981	Stark			
	A35 4 5 8 6 1 6 3	1986	Koike			
	A36 4 6 5 3 0 2 3	1987	Suzuki et al.			
	A37 4 8 4 7 8 0 8	1989	Kobatake			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

C21	Stark, M., "Two Bits Per Cell Rom," <u>IEEE Catalog No. 81-CH1626-1</u> , Library of Congress No. 80-85186, Order No. 341, Spring Comp Con 1981, Feb. 23-26, Twenty-Second Computer Society International Conference, San Francisco, CA
C22	Furuyama et al., "An Experimental 2-Bit/Cell Storage Dram For Macro Cell Or Memory-On-Logic Application," pp. 4.4.1 - 4.4.4, <u>IEEE</u> , (1988)
C23	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16 Levels Cell Storage," <u>IEEE Journal Of Solid-State Circuits</u> , Vol. 23, No. 1, February 1988

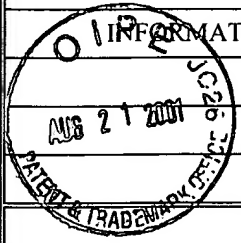
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Sheet 1 of 1

U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					11587 M-10187-43C US		09/867,836	
					Applicant(s)			
(Use several sheets if necessary)					Eliyahou Harari et al.			
					Filing Date		Group	
					May 30, 2001		2824	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,991,517	Nov. 23, 1999	Harari et al.				
	AB							
	AC							
	AD							
	AL							
	AF							
	AG							
	AH							
	AI							
	AJ							
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL	60-15896	Jan. 26, 1985	Japan			Yes	
	AM	62-188100	Aug. 17, 1987	Japan			Yes	
	AN	62-52798	Mar. 7, 1987	Japan			Abstract	
	AO	62-76098	Apr. 8, 1987	Japan			Abstract	
	AP	62-80899	Apr. 14, 1987	Japan			Abstract	
	AQ	63-291294	Nov. 29, 1988	Japan			Abstract	
	AR							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AS							
	AT							
Examiner			Date Considered					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								